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NOV 22 2006IN THE CLAIMS:

1. (Currently Amended) A nonvolatile memory semiconductor device comprising:
 - a memory cell array including a plurality of memory cells being formed in a matrix;
 - wherein at least one of the memory cells comprises:
 - a memory thin film transistor; and
 - a switching thin film transistor;
 - wherein said a memory thin film transistor comprises comprising:
 - a first semiconductor active layer comprising a channel forming region over an insulating surface;
 - a layer adjacent to the first semiconductor active layer with a first insulating film therebetween; and
 - a control gate electrode adjacent to the floating gate layer with a second insulating film therebetween;
 - wherein said switching thin film transistor comprises:
 - a second semiconductor active layer over the insulating surface; and
 - a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween;
 - wherein the first semiconductor active layer and the second semiconductor active layer are in a common semiconductor island;
 - wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer of the switching thin film transistor;
 - wherein the layer adjacent to the first semiconductor active layer traps electrons;
 - wherein the control gate is a laminate film comprising a first film[,] and a second film and a third film;
 - wherein the first film comprises tantalum nitride;
 - wherein the second film comprises tungsten; and
 - wherein the first film and the second film comprises an inert element
 - ~~wherein the third film comprises tungsten nitride.~~

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2-76. (Canceled)

77. (Currently Amended) A semiconductor device comprising[[:]]

~~a substrate;~~~~a non-volatile memory over the substrate;~~~~a pixel portion over the substrate;~~~~a source wiring driver circuit for driving the pixel portion over the substrate;~~~~a gate wiring driver circuit for driving the pixel portion over the substrate; and~~~~a correction circuit over the substrate;~~~~wherein the non-volatile memory comprises a plurality of memory cells;~~~~wherein at least one of the memory cells comprises:~~~~a memory thin film transistor; and~~~~a switching thin film transistor;~~~~wherein said a memory thin film transistor comprises comprising:~~~~a first semiconductor active layer comprising a channel forming region over an insulating surface;~~~~a layer floating gate electrode adjacent to the first semiconductor active layer with a first insulating film therebetween;~~~~a control gate electrode adjacent to the floating gate electrode with a second insulating film therebetween,~~~~wherein said switching thin film transistor comprises:~~~~a second semiconductor active layer over the insulating surface; and~~~~a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween;~~~~wherein the first semiconductor active layer and the second semiconductor active layer are in a common semiconductor island;~~~~wherein the layer adjacent to the first semiconductor active layer traps electrons;~~~~wherein the control gate is a laminate film comprising a first film[[:]] and a second film and a third film,~~~~wherein the first film comprises tantalum nitride,~~~~wherein the second film comprises tungsten, and~~

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wherein the first film and the second film comprises an inert element
~~wherein the third film comprises tungsten nitride.~~

78. (Currently Amended) A semiconductor device comprising:
a substrate having an insulating surface;
a non-volatile memory over the substrate;
a pixel portion;
a source wiring driver circuit for driving the pixel portion over the substrate;
a gate wiring driver circuit for driving the pixel portion over the substrate; and
~~a memory controller circuit over the substrate for controlling the non-volatile memory~~
~~circuit,~~
wherein the non-volatile memory comprises a plurality of memory cells,
~~wherein at least one of the memory cells comprises:~~
~~a memory thin film transistor; and~~
~~a switching thin film transistor;~~
~~wherein said a memory thin film transistor comprises~~ comprising:
a first semiconductor active layer comprising a channel forming region over ~~over~~ the
insulating surface;
a layer adjacent to the first semiconductor active layer with a first insulating film
therebetween; and
a control gate electrode adjacent to the floating gate electrode layer with a second
insulating film therebetween,
~~wherein said switching thin film transistor comprises:~~
~~a second semiconductor active layer over the insulating surface; and~~
~~a gate electrode adjacent to the second semiconductor active layer with a gate~~
~~insulating film therebetween;~~
~~wherein the first semiconductor active layer and the second semiconductor active layer~~
~~are in a common semiconductor island;~~
wherein the layer adjacent to the first semiconductor active layer traps electrons,
wherein the control gate is a laminate film comprising a first film and a second
film ~~and a third film,~~

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wherein the first film comprises tantalum nitride,
wherein the second film comprises tungsten, and
wherein the first film and the second film comprises an inert element
~~wherein the third film comprises tungsten nitride.~~

79. (Currently Amended) A semiconductor device comprising[[:]]

~~a substrate;~~

~~a non-volatile memory over the substrate;~~

~~a pixel portion over the substrate;~~

~~a source wiring driver circuit for driving the pixel portion over the substrate;~~

~~a gate wiring driver circuit for driving the pixel portion over the substrate; and~~

~~a correction circuit over the substrate;~~

~~wherein the non-volatile memory comprises comprising:~~

an X-address decoder;

a Y-address decoder;

n first signal lines electrically connected to the X-address decoder;

m second signal lines electrically connected to the Y-address decoder;

m third signal lines electrically connected to the Y-address decoder; and

a plurality of memory cells;

~~wherein at least one of the memory cells comprises:~~

~~a memory thin film transistor; and~~

~~a switching thin film transistor;~~

wherein said n x m memory thin film transistor transistors arranged in a matrix, each
of which comprises:

a first semiconductor active layer over an insulating surface, comprising a channel
forming region, a source region electrically connected to corresponding one of the m second
signal lines, and a drain region electrically connected to corresponding one of the m third
signal lines over an insulating surface;

a layer adjacent to the first semiconductor active layer with a first insulating film
therebetween; and

a control gate electrode electrically connected to corresponding one of the n first signal

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lines, adjacent to the floating gate electrode layer with a second insulating film therebetween,
wherein said switching thin film transistor comprises:
a second semiconductor active layer over the insulating surface; and
a gate electrode adjacent to the second semiconductor active layer with a gate
insulating film therebetween;
wherein the first semiconductor active layer and the second semiconductor active
layer are in a common semiconductor island;
wherein a first thickness of the first semiconductor active layer of the memory thin
film transistor is thinner than a second thickness of the second semiconductor active layer of
the switching thin film transistor;
wherein n and m are natural numbers;
wherein the layer adjacent to the first semiconductor active layer traps electrons,
wherein the control gate is a laminate film comprising a first film $[[,]]$ and a second
film and a third film;
wherein the first film comprises tantalum nitride,
wherein the second film comprises tungsten, and
wherein the first film and the second film comprises an inert element
wherein the third film comprises tungsten nitride.

80. (Currently Amended) A semiconductor device comprising $[[:]$

a substrate;
a non-volatile memory over the substrate;
a pixel portion;
a source wiring driver circuit for driving the pixel portion over the substrate;
a gate wiring driver circuit for driving the pixel portion over the substrate; and
a memory controller circuit over the substrate for controlling the non-volatile memory
circuit;
wherein the non-volatile memory comprises comprising:
an X-address decoder;
a Y-address decoder;
n first signal lines electrically connected to the X-address decoder;

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m second signal lines electrically connected to the Y-address decoder;
m third signal lines electrically connected to the Y-address decoder; and
a plurality of memory cells;
wherein at least one of the memory cells comprises:
a memory thin film transistor; and
a switching thin film transistor;
wherein said n x m memory thin film transistor transistors arranged in a matrix, each
of which comprises:
a first semiconductor active layer over an insulating surface, comprising a channel
forming region, a source region electrically connected to corresponding one of the m second
signal lines, and a drain region electrically connected to corresponding one of the m third
signal lines over an insulating surface;
a floating gate electrode adjacent to the first semiconductor active layer with a first
insulating film therebetween; and
a control gate electrode electrically connected to corresponding one of the n first signal
lines, adjacent to the floating gate electrode with a second insulating film therebetween,
wherein said switching thin film transistor comprises:
a second semiconductor active layer over the insulating surface; and
a gate electrode adjacent to the second semiconductor active layer with a gate
insulating film therebetween;
wherein the first semiconductor active layer and the second semiconductor active layer
are in a common semiconductor island;
wherein a first thickness of the first semiconductor active layer of the memory thin
film transistor is thinner than a second thickness of the second semiconductor active layer of
the switching thin film transistor;
wherein the layer adjacent to the first semiconductor active layer traps electrons;
wherein n and m are natural numbers.
wherein the control gate is a laminate film comprising a first film[.] and a second
film and a third film,
wherein the first film comprises tantalum nitride,
wherein the second film comprises tungsten, and

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wherein the first film and the second film comprises an inert element
~~wherein the third film comprises tungsten nitride.~~

81. (Currently Amended) A semiconductor device according to claim 77,
~~wherein the floating gate electrode comprises one of tantalum and tantalum alloy, and~~
wherein the second insulating film comprises a thermal an oxide film of the floating
gate electrode.

82. (Currently Amended) A semiconductor device according to claim 78,
~~wherein the floating gate electrode comprises one of tantalum and tantalum alloy, and~~
wherein the second insulating film comprises a thermal an oxide film of the floating
gate electrode.

83. (Currently Amended) A semiconductor device according to claim 79,
~~wherein the floating gate electrode comprises one of tantalum and tantalum alloy, and~~
wherein the second insulating film comprises a thermal an oxide film of the floating
gate electrode.

84. (Currently Amended) A semiconductor device according to claim 80,
~~wherein the floating gate electrode comprises one of tantalum and tantalum alloy, and~~
wherein the second insulating film comprises a thermal an oxide film of the floating
gate electrode.

85-86. (Canceled)

87. (Previously Presented) A semiconductor device according to claim 77,
wherein the semiconductor device is one selected from the group consisting of a liquid
crystal display device and an EL display device.

88. (Previously Presented) A semiconductor device according to claim 78,
wherein the semiconductor device is one selected from the group consisting of a liquid

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crystal display device and an EL display device.

89. **(Previously Presented)** A semiconductor device according to claim 79, wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

90. **(Previously Presented)** A semiconductor device according to claim 80, wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

91-92. **(Canceled)**

93. **(Previously Presented)** A semiconductor device according to claim 77, wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

94. **(Previously Presented)** A semiconductor device according to claim 78, wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

95. **(Previously Presented)** A semiconductor device according to claim 79, wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

96. **(Previously Presented)** A semiconductor device according to claim 80, wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

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97. (Currently Amended) A ~~nonvolatile memory~~ semiconductor device according to claim 1, ~~wherein the first and the second semiconductor active layers contain amorphous silicon-germanium~~

wherein a laminate film further comprises a third film, and
wherein the third film comprises tungsten nitride and an inert element.

98. (Currently Amended) A semiconductor device according to claim 77, ~~wherein the first and the second semiconductor active layers contain amorphous silicon-germanium~~

wherein a laminate film further comprises a third film, and
wherein the third film comprises tungsten nitride and an inert element.

99. (Currently Amended) A semiconductor device according to claim 78, ~~wherein the first and the second semiconductor active layers contain amorphous silicon-germanium~~

wherein a laminate film further comprises a third film, and
wherein the third film comprises tungsten nitride and an inert element.

100. (Currently Amended) A semiconductor device according to claim 79, ~~wherein the first and the second semiconductor active layers contain amorphous silicon-germanium~~

wherein a laminate film further comprises a third film, and
wherein the third film comprises tungsten nitride and an inert element.

101. (Currently Amended) A semiconductor device according to claim 80, ~~wherein the first and the second semiconductor active layers contain amorphous silicon-germanium~~

wherein a laminate film further comprises a third film, and
wherein the third film comprises tungsten nitride and an inert element.

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102. (Currently Amended) A ~~nonvolatile memory~~ semiconductor device according to claim 1, ~~the layer adjacent to the first semiconductor active layer comprises one of tantalum and tantalum alloy, and~~

wherein the second insulating film comprises a thermal ~~an~~ oxide film ~~of the floating gate electrode.~~

103. (Currently Amended) A ~~nonvolatile memory~~ semiconductor device according to claim 1, wherein the layer adjacent to the first semiconductor active layer is an electrically conductive layer.

104. (Canceled)

105. (Currently Amended) A semiconductor device according to claim 78, wherein the layer adjacent to the first semiconductor active layer is an electrically conductive layer.

106. (Currently Amended) A semiconductor device according to claim 79, wherein the layer adjacent to the first semiconductor active layer is an electrically conductive layer.

107. (Canceled)

108. (New) A semiconductor device according to claim 1, wherein the semiconductor device is one selected from the group consisting of a liquid crystal display device and an EL display device.

109. (New) A semiconductor device according to claim 1, wherein the semiconductor device is one selected from the group consisting of a display, a video camera, a head-mounted type display, a DVD display, a goggle type display, a personal computer, a portable telephone, and a car audio.

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110. (New) A semiconductor device according to claim 1, wherein the inert element is xenon.

111. (New) A semiconductor device according to claim 77, wherein the inert element is xenon.

112. (New) A semiconductor device according to claim 78, wherein the inert element is xenon.

113. (New) A semiconductor device according to claim 79, wherein the inert element is xenon.

114. (New) A semiconductor device according to claim 80, wherein the inert element is xenon.

115. (New) A semiconductor device according to claim 77, wherein the floating gate comprises silicon to which one conductivity is imparted.

116. (New) A semiconductor device according to claim 80, wherein the floating gate comprises silicon to which one conductivity is imparted.

117. (New) A semiconductor device according to claim 1, further comprising:
a switching thin film transistor comprising:
a second semiconductor active layer over the insulating surface; and
a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island, and

wherein a first thickness of the semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer.

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118. (New) A semiconductor device according to claim 77, further comprising:
a switching thin film transistor comprising:
a second semiconductor active layer over the insulating surface; and
a gate electrode adjacent to the second semiconductor active layer with a gate
insulating film therebetween,
wherein the semiconductor active layer of the memory thin film transistor and the
second semiconductor active layer are in a common semiconductor island, and
wherein a first thickness of the semiconductor active layer of the memory thin film
transistor is thinner than a second thickness of the second semiconductor active layer.

119. (New) A semiconductor device according to claim 78,
wherein the non-volatile memory further comprises:
a switching thin film transistor comprising:
a second semiconductor active layer over the insulating surface; and
a gate electrode adjacent to the second semiconductor active layer with a gate
insulating film therebetween,
wherein the semiconductor active layer of the memory thin film transistor and the
second semiconductor active layer are in a common semiconductor island, and
wherein a first thickness of the semiconductor active layer of the memory thin film
transistor is thinner than a second thickness of the second semiconductor active layer.

120. (New) A semiconductor device according to claim 79,
wherein the non-volatile memory further comprises:
 $n \times m$ switching thin film transistors, each of which comprising:
a second semiconductor active layer over the insulating surface; and
a gate electrode adjacent to the second semiconductor active layer with a gate
insulating film therebetween,
wherein the semiconductor active layer of the memory thin film transistor and the
second semiconductor active layer are in a common semiconductor island, and
wherein a first thickness of the semiconductor active layer of the memory thin film
transistor is thinner than a second thickness of the second semiconductor active layer.

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121. (New) A semiconductor device according to claim 80,
wherein the non-volatile memory further comprises:
n x m switching thin film transistors, each of which comprising:
a second semiconductor active layer over the insulating surface; and
a gate electrode adjacent to the second semiconductor active layer with a gate
insulating film therebetween,
wherein the semiconductor active layer of the memory thin film transistor and the
second semiconductor active layer are in a common semiconductor island, and
wherein a first thickness of the semiconductor active layer of the memory thin film
transistor is thinner than a second thickness of the second semiconductor active layer.

122. (New) A semiconductor device comprising a memory thin film transistor
comprising:
a semiconductor active layer comprising a channel forming region;
a layer adjacent to the semiconductor active layer with a first insulating film
therebetween; and
a control gate electrode adjacent to the layer with a second insulating film
therebetween,
wherein the layer adjacent to the semiconductor active layer traps electrons,
wherein the control gate is a laminate film comprising a first film and a second film,
wherein the first film comprises tantalum nitride,
wherein the second film comprises tungsten, and
wherein the first film and the second film comprises an inert element.

123. (New) A semiconductor device comprising a memory thin film transistor
comprising:
a semiconductor active layer comprising a channel forming region;
a floating gate electrode adjacent to the semiconductor active layer with a first
insulating film therebetween;
a control gate electrode adjacent to the floating gate electrode with a second insulating

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film therebetween,

wherein the control gate is a laminate film comprising a first film and a second film,
wherein the first film comprises tantalum nitride,
wherein the second film comprises tungsten, and
wherein the first film and the second film comprises an inert element.

124. (New) A semiconductor device comprising a non-volatile memory comprising:

an X-address decoder;
a Y-address decoder;
n first signal lines electrically connected to the X-address decoder;
m second signal lines electrically connected to the Y-address decoder;
m third signal lines electrically connected to the Y-address decoder; and
n x m memory thin film transistors arranged in a matrix, each of which comprises:
a semiconductor active layer comprising a channel forming region, a source region electrically connected to corresponding one of the m second signal lines, and a drain region electrically connected to corresponding one of the m third signal lines;
a layer adjacent to the semiconductor active layer with a first insulating film therebetween; and
a control gate electrode electrically connected to corresponding one of the n first signal lines, adjacent to the layer with a second insulating film therebetween,
wherein n and m are natural numbers,
wherein the layer adjacent to the semiconductor active layer traps electrons,
wherein the control gate is a laminate film comprising a first film and a second film,
wherein the first film comprises tantalum nitride,
wherein the second film comprises tungsten, and
wherein the first film and the second film comprises an inert element.

125. (New) A semiconductor device comprising a non-volatile memory comprising:

an X-address decoder;

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a Y-address decoder;
n first signal lines electrically connected to the X-address decoder;
m second signal lines electrically connected to the Y-address decoder;
m third signal lines electrically connected to the Y-address decoder; and
n x m memory thin film transistors arranged in a matrix, each of which comprises:
a semiconductor active layer comprising a channel forming region, a source region
electrically connected to corresponding one of the m second signal lines, and a drain region
electrically connected to corresponding one of the m third signal lines;
a floating gate electrode adjacent to the semiconductor active layer with a first
insulating film therebetween; and
a control gate electrode electrically connected to corresponding one of the n first signal
lines, adjacent to the floating gate electrode with a second insulating film therebetween,
wherein n and m are natural numbers,
wherein the control gate is a laminate film comprising a first film and a second film,
wherein the first film comprises tantalum nitride,
wherein the second film comprises tungsten, and
wherein the first film and the second film comprises an inert element.

126. (New) A semiconductor device according to claim 122, wherein the second
insulating film comprises an oxide film.

127. (New) A semiconductor device according to claim 123, wherein the second
insulating film comprises an oxide film.

128. (New) A semiconductor device according to claim 124, wherein the second
insulating film comprises an oxide film.

129. (New) A semiconductor device according to claim 125, wherein the second
insulating film comprises an oxide film.

130. (New) A semiconductor device according to claim 122,

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wherein a laminate film further comprises a third film, and
wherein the third film comprises tungsten nitride and an inert element.

131. (New) A semiconductor device according to claim 123,
wherein a laminate film further comprises a third film, and
wherein the third film comprises tungsten nitride and an inert element.

132. (New) A semiconductor device according to claim 124,
wherein a laminate film further comprises a third film, and
wherein the third film comprises tungsten nitride and an inert element.

133. (New) A semiconductor device according to claim 125,
wherein a laminate film further comprises a third film, and
wherein the third film comprises tungsten nitride and an inert element.

134. (New) A semiconductor device according to claim 122,
wherein the semiconductor device is one selected from the group consisting of a liquid
crystal display device and an EL display device.

135. (New) A semiconductor device according to claim 123,
wherein the semiconductor device is one selected from the group consisting of a liquid
crystal display device and an EL display device.

136. (New) A semiconductor device according to claim 124,
wherein the semiconductor device is one selected from the group consisting of a liquid
crystal display device and an EL display device.

137. (New) A semiconductor device according to claim 125,
wherein the semiconductor device is one selected from the group consisting of a liquid
crystal display device and an EL display device.

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138. (New) A semiconductor device according to claim 122,
wherein the semiconductor device is one selected from the group consisting of a
display, a video camera, a head-mounted type display, a DVD display, a goggle type display,
a personal computer, a portable telephone, and a car audio.

139. (New) A semiconductor device according to claim 123,
wherein the semiconductor device is one selected from the group consisting of a
display, a video camera, a head-mounted type display, a DVD display, a goggle type display,
a personal computer, a portable telephone, and a car audio.

140. (New) A semiconductor device according to claim 124,
wherein the semiconductor device is one selected from the group consisting of a
display, a video camera, a head-mounted type display, a DVD display, a goggle type display,
a personal computer, a portable telephone, and a car audio.

141. (New) A semiconductor device according to claim 125,
wherein the semiconductor device is one selected from the group consisting of a
display, a video camera, a head-mounted type display, a DVD display, a goggle type display,
a personal computer, a portable telephone, and a car audio.

142. (New) A semiconductor device according to claim 122, wherein the layer
adjacent to the semiconductor active layer is an electrically conductive layer.

143. (New) A semiconductor device according to claim 124, wherein the layer
adjacent to the semiconductor active layer is an electrically conductive layer.

144. (New) A semiconductor device according to claim 122, wherein the inert
element is xenon.

145. (New) A semiconductor device according to claim 123, wherein the inert
element is xenon.

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146. (New) A semiconductor device according to claim 124, wherein the inert element is xenon.

147. (New) A semiconductor device according to claim 125, wherein the inert element is xenon.

148. (New) A semiconductor device according to claim 123, wherein the floating gate comprises silicon to which one conductivity is imparted.

149. (New) A semiconductor device according to claim 125, wherein the floating gate comprises silicon to which one conductivity is imparted.

150. (New) A semiconductor device according to claim 122, further comprising:
a switching thin film transistor comprising:
a second semiconductor active layer over the insulating surface; and
a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island, and

wherein a first thickness of the semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer.

151. (New) A semiconductor device according to claim 123, further comprising:
a switching thin film transistor comprising:
a second semiconductor active layer over the insulating surface; and
a gate electrode adjacent to the second semiconductor active layer with a gate insulating film therebetween,

wherein the semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are in a common semiconductor island, and

wherein a first thickness of the semiconductor active layer of the memory thin film

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transistor is thinner than a second thickness of the second semiconductor active layer.

152. (New) A semiconductor device according to claim 124,
wherein the non-volatile memory further comprises:
n x m switching thin film transistors, each of which comprising:
a second semiconductor active layer over the insulating surface; and
a gate electrode adjacent to the second semiconductor active layer with a gate
insulating film therebetween,
wherein the semiconductor active layer of the memory thin film transistor and the
second semiconductor active layer are in a common semiconductor island, and
wherein a first thickness of the semiconductor active layer of the memory thin film
transistor is thinner than a second thickness of the second semiconductor active layer.

153. (New) A semiconductor device according to claim 125,
wherein the non-volatile memory further comprises:
n x m switching thin film transistors, each of which comprising:
a second semiconductor active layer over the insulating surface; and
a gate electrode adjacent to the second semiconductor active layer with a gate
insulating film therebetween,
wherein the semiconductor active layer of the memory thin film transistor and the
second semiconductor active layer are in a common semiconductor island, and
wherein a first thickness of the semiconductor active layer of the memory thin film
transistor is thinner than a second thickness of the second semiconductor active layer.

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